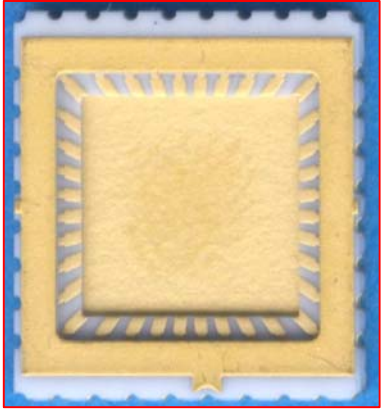
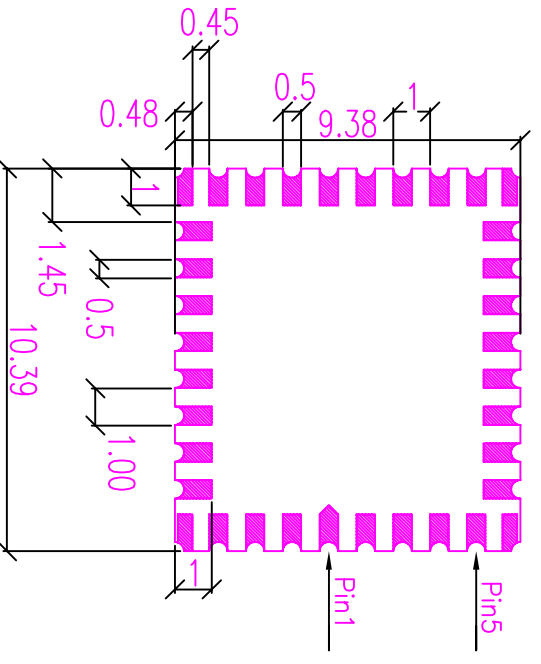
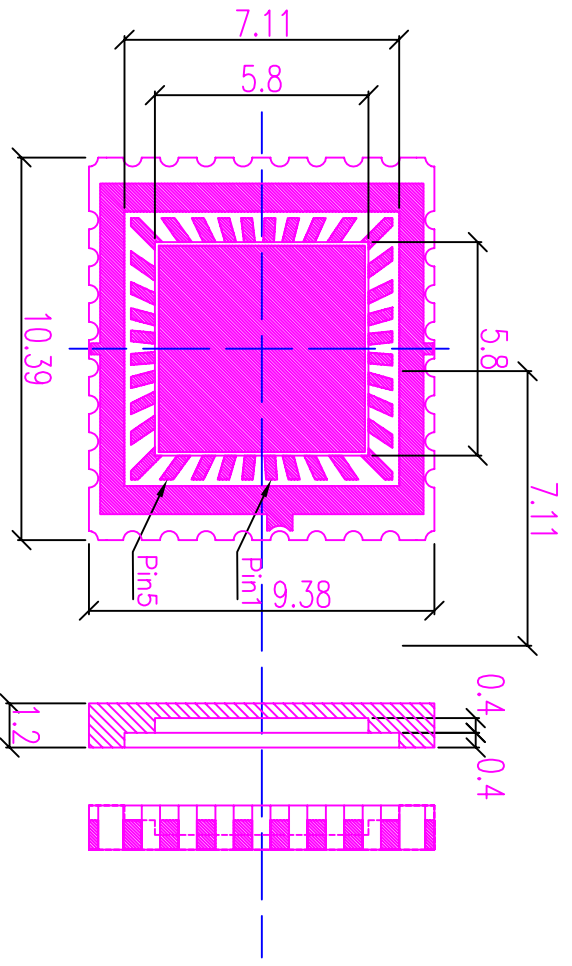
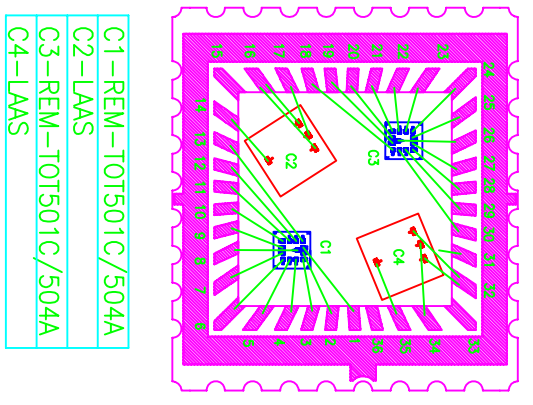


Part Dimensions
36 pin square Ceramic Chip Carrier
MIL-STD-105 D



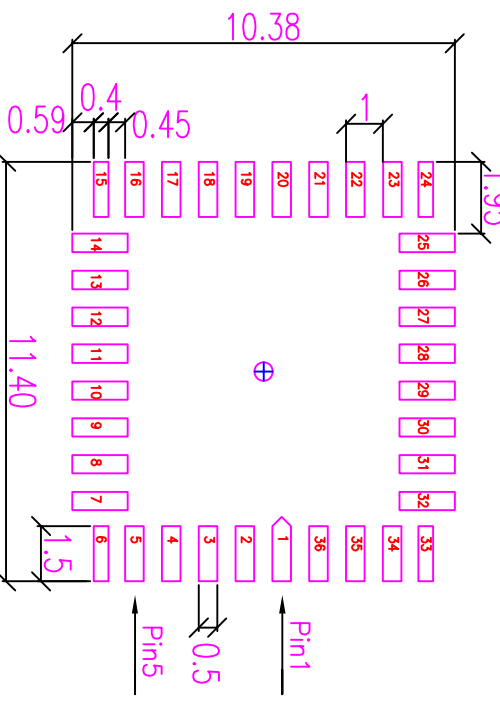
Part bounding (Model 0)

01-C1-D3-K	19-C3-D3-K
02-C1-S2-K	20-C3-S2-K
03-C1-G2-K	21-C3-G2-K
04-C1-D2-K	22-C3-D2-K
05-C1-S1-R	23-C3-S1-R
06-C1-G1-R	24-C3-G1-R
07-C1-D1-R	25-C3-D1-R
08-C1-BULK	26-C3-BULK
09-C1-S4-R	27-C3-S4-R
10-C1-G4-R	28-C3-G4-R
11-C1-D4-R	29-C3-D4-R
12-C1-S3-K	30-C3-S3-K
13-C1-G3-K	31-C2C4-BULK
14-C2-S	32-C4-G
15-FREE	33-FREE
16-C2-G	34-C4-D
17-C2-D	35-C4-S
18-C3-G3-K	36-FREE



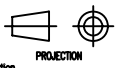
C1-REM-TOT501C/504A
C2-LAAS
C3-REM-TOT501C/504A
C4-LAAS

Land pattern LDCC36 (Model 0)



1	Kioxia 36LDC 9.38 x 10.38 x 1.2 mm	1	Ceramic Metallization W or equivalent
QUANT.	Specification: AS-1003-A	POS	Kioxia A-473 Lead frame 42 Alloy Gold plating 91.9% 1.5 um
ENS/ASS		MAT.	
Chip carrier for REM-LAAS MOSFET disintegraters		S.ENS/S.ASS	
RADMON		SCHEDULE	10:1
36LD Chip Carrier		DES/DIR.	M. Gaiser 17/06/2005
		APPRO.	
		REPLACE/REPLACES	PH-DT2-SD 07/05/2005
			F-0012 0

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DESSIN, RUGOSITE, TOLERANCES SELON NORMES ISO
DRAWING, RUGOSITY, TOLERANCES ACCORDING TO ISO STANDARDS

DIMENSION	<=6	> 6	> 30	> 120	> 315	>1000	>2000
USINAGE MOYEN/MEDIUM MACHINING	± 0.1	± 0.2	± 0.3	± 0.5	± 0.8	± 1.2	± 2
MECAN. SOUDURE/WELDED STRUCTURE	± 0.5	± 1	± 2	± 3	± 5	± 7	± 10

11 10 9 8 7 6 5 4 3 2 1